main electrode, the gate electrode, and the second main electrode, and a diode region in which a Schottky diode is formed between the first main electrode and the second main electrode;

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, a first end of the inner lead frame being connected to the main electrode on at least a part of the diode region, a second end of the inner lead frame being connected to a package lead.

25. (New) The semiconductor device according to claim 24, wherein the first end of the inner lead frame covers the diode region entirely.

26. (New) The semiconductor device according to claim 24, wherein the transistor chip includes an N-channel MOSFET.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 8-26 are pending in this application. Withdrawn Claims 1-7 have been cancelled by the present response without prejudice. Claims 21-26 are added by the present response. Claim 11 was rejected under 35 U.S.C. § 112, first paragraph. Claims 8, 10, 11, and 14 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent no. 6,144,093 to Davis et al. (herein "Davis"). Claims 8, 12, and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Davis in view of U.S. patent no. 6,229,205 to Jeong et al. (herein "Jeong").

Claims 8 and 9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Davis in view of U.S. patent no. 5,859,471 to Kuraishi et al. (herein "Kuraishi")[2]. Claims 15-20 are allowed.

Initially, applicant gratefully acknowledges the early indication of the allowance of Claims 15-20.

Addressing now the rejection of Claim 11 under 35 U.S.C. § 112, first paragraph, that rejection is traversed by the present response.

Claim 11 is amended by the present response to clarify that the "tie bar comprises a plurality of sub tie bars connecting between the two inner leads and arranged separately". That subject matter is supported by the original specification for example in Figures 5 and 6, elements 19b, 19b', 19c, and 19c'. As shown in those figures, each tie bar includes plural sub tie bars.

In view of the presently submitted amendment to Claim 11 and the above-noted comments, Claim 11 is believed to be in full compliance with all requirements under 35 U.S.C. § 112, first paragraph.

Addressing now the rejection of Claims 8, 10, 11, and 14 under 35 U.S.C. § 102(e) as anticipated by Davis, that rejection is traversed by the present response.

It is initially noted that Claim 8 is amended by the present response to clarify features recited therein. Specifically, Claim 8 now clarifies that the two inner leads each have "a portion of a cut remainder of a tie bar". That claim amendment is believed to merely clarify the language originally recited in Claim 8, and thus the claim amendment is not believed to narrow Claim 8 in any aspect.

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[2]This grounds for rejection stated on page 5 of the Office Action references Claims 1 and 9, although that appears to be a typographical error and the rejection appears to properly be directed to Claims 8 and 9.

Claim 1 is directed to a semiconductor device in which before a lead frame is integrated in the semiconductor device, leads of the lead frame are joined together by a tie bar. The tie bar is shown, as non-limiting examples, as element 19 in Figures 1A and 3, and as element 19b, 19b', 19c, 19c', in Figures 5 and 6 in the present specification.

With reference to Figure 1A, the lead frame on the left side of Figure 1A shows that the tie bar 19 is cut in the area between the dashed lines. As a result, after the tie bar 19 is cut each of the inner leads 15, 17 has a portion of a cut remainder of the tie bar 19. Such a feature also is believed to distinguish over the teachings in Davis.

The inner leads 44, 46 described in Davis are not formed in the form of a lead frame, and therefore neither of them has a portion of a cut remainder of a tie bar. Therefore, independent Claim 8, and the claims dependent therefrom, are believed to distinguish over the teachings in Davis.

Addressing now the rejection of Claims 8, 12, and 13 under 35 U.S.C. § 103(a) as unpatentable over Davis in view of Jeong, that rejection is also traversed by the present response.

Jeong does not overcome the above-noted deficiencies in Davis. Moreover, the notch described in Jeong does not face a tie bar. Moreover, the tie bars 46, 47 shown in Figure 3B of Jeong are not formed higher than an upper surface of the semiconductor chip 90.

In such ways, Claims 8, 12, and 13 are believed to distinguish over the teachings of Davis in view of Jeong.

Addressing now the rejection of Claims 8 and 9 under 35 U.S.C. § 103(a) as unpatentable over Davis in view of Kuraishi, that rejection is also traversed by the present response.

The deficiencies of Davis are discussed above. Further, Kuraishi cannot overcome the deficiencies in Davis.

Moreover, Figure 1B of Kuraishi is a plan view and thus that view does not provide any indication of a thickness of a tie bar relative to other portions of inner leads. Further, even at column 4, lines 58-63, Kuraishi is silent as to any relationship of thickness as recited in Claim 9.

Thus, Claims 8 and 9 also distinguish over the combination of teachings in Davis in view of Kuraishi.

The present response also sets forth new Claims 21-26 for examination. New Claims 21-26 are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter. Further, new Claims 21-26 are directed to semiconductor devices, such as vertical transistors, shown as non-limiting examples in Figure 7A-7C and 8 in the present specification. New Claims 21-26 are also believed to recite allowable subject matter.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

--8. (Amended) A semiconductor device comprising:

a plurality of external leads;

a die pad adjacent to the plurality of external leads;

a semiconductor chip mounted on the die pad and having a main electrode and a subelectrode smaller in area than the main electrode;

two inner leads [for connecting] configured to connect the main electrode and the subelectrode on the semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, the two inner leads each having a portion of a cut remainder of a tie bar [cut].

11. (Amended) The semiconductor device according to claim 8, wherein the tie bar [has] comprises a plurality of sub tie bars connecting between the two inner leads and arranged separately.

12. (Amended) The semiconductor device according to claim 8, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar.

15. (Amended) A semiconductor device comprising:

a plurality of external leads;

a first and a second die pad placed side by side adjacent to the plurality of external leads;

a first and a second semiconductor chip each having a main electrode and a subelectrode smaller in area than the main electrode;

two pairs of inner leads [for connecting] configured to connect the main electrode and the subelectrode on each of the first and the second semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, each pair of the inner leads having a portion of a cut remainder of a tie bar [cut];

a protruding lead portion formed vertically on one side of the first die pad which faces the second die pad; and

reason for allowance

a connecting lead portion formed integrally with one of the inner leads which is connected to the main electrode on the second semiconductor chip mounted on the second die pad and having a notch engaged with the protruding lead portion so that the connecting lead portion and the protruded lead portion are electrically joined together.

20. (Amended) The semiconductor device according to claim 15, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar.

Claims 21-26 (New).--